Technical Note

Upgrating Semiconductors for High-Temperature Applications

Introduction

Uprating is used to evaluate a semiconductor component's ability to function and perform when used outside of the manufacturer's specified temperature range[21].

Before operating a DRAM component above its maximum specified temperature, a customer can use the uprating process to determine the related risks. Uprating is possible because semiconductor manufacturers design margin into their products to increase device yield and reliability. Through its commercial off-the-shelf (COTS) program, the U.S. Department of Defense has been uprating for a number of years. Three major concerns are associated with uprating:

- Device functionality and performance to data sheet specifications
- Device reliability
- Package reliability

This technical note describes the issues associated with temperature uprating and the risks involved in using components outside the manufacturers' environmental specifications. It focuses specifically on temperature uprating and the significant failure mechanisms associated with operating semiconductors outside their specified temperature ranges. The failure mechanisms apply to all semiconductor products, whether manufactured by Micron or any other semiconductor company.

Device Functionality

Micron semiconductor devices go through a series of functional tests under elevated temperatures to ensure device performance. The device temperature specifications are derived directly from these tests. Table 1 shows the industry standard temperature definitions for CMOS-based devices. If these temperatures are exceeded, the data sheet specifications cannot be guaranteed. As with all semiconductor devices, increasing temperatures adversely affects device operation and reliability. Even though all Micron devices have margin, Micron cannot guarantee data sheet compliance or reliability if the specifications are exceeded.

Junction Temperature, Functionality

See Micron's Thermal Applications Technical Note (TN-00-08) for junction temperature limits and Micron product data sheets for product temperature specifications.

Table 1: Industry Standard Typical Temperature Limits

Application	Temperature (°C)	
	MIN	MAX
Commercial	0	70
Industrial	-40	95
Automotive		
- Grade 0	-40	150
- Grade 1	-40	125
- Grade 2	-40	105
- Grade 3	-40	85
- Grade 4	0	70
Military (example of one range)	-65	125

Device Reliability

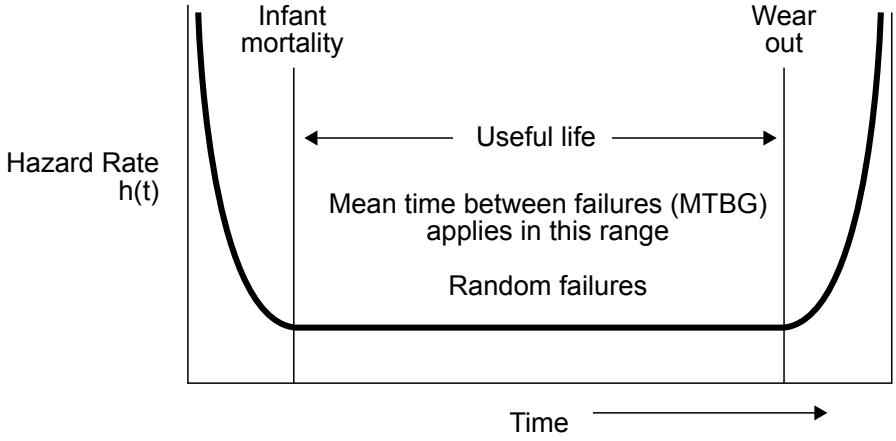
When determining the risk associated with operating at extended temperatures, a few factors must be considered:

- What is the real reliability target of the end system?
- What is the useful life of the end system? (For example, if the end system is a GPS navigation system for a car, how long does the unit need to last?)
- How many hours a day will the unit be powered throughout its life?

If you assume 2 hours of use a day across a 20-year life, the DRAM only has to last 14,560 hours, or about 1.7 years of continuous use assuming only 1 DRAM per system. The values determined in the failure in time per billion device hours (FIT) rate calculations only apply when there is power to the device. In most cases, the functional life of the end system is far shorter than that of the DRAM, primarily because the reliability standards that govern the DRAM industry are based on applications that use 32 or more devices per system, such as servers. The number of devices in the system and their effects on reliability are detailed in the Failure Rate Calculation section later in this document.

The long-term reliability and failure rates for CMOS devices is typically described in the form of a curve depicting the life of the IC. This reliability curve is known as a bathtub curve due to its shape (see the figure below). The curve shows the failure rate of a population of ICs over time. A small percentage of devices will have inherent manufacturing defects after the devices have passed all electrical testing and are functional at time = 0. Manufacturing defects caused by contamination and process variation lead to a shorter life in comparison to the remaining population. These defects are referred to as "infant mortality." Infant mortality makes up only a small percentage of the total population, but is the largest percentage of early life failures in ICs.

Figure 1: Reliability Curve



DRAM devices are subjected to 125°C at elevated voltages (burn-in) to remove the infant mortality part of the population prior to shipping. After the devices in the infant mortality section of the bathtub curve are removed from the population, the remaining part of the population displays a stable field failure rate. Micron uses an intelligent burnin — the parts are operated during the stress condition to show the exact time of failure. Following the infant mortality section, there is a relatively flat portion of the bathtub curve that represents the useful life of the IC, where you would expect to see a very low field failure rate. The random field failures experienced during the useful life of the IC will eventually be replaced with an exponential failure rate. This is shown in the wear out section of the bathtub curve. The time frame and random field failures in the useful life of the IC can be predicted using statistics based on lab data from a sample of parts and will vary greatly depending on the operating temperature the IC. This process is explained in detail in the following pages.

Long-Term Reliability

Statistically predicting the long-term reliability of a DRAM requires test conditions that accelerate the stress on the device to screen out those with defects, while at the same time not damaging the remaining portion of the population. Both temperature and voltage are used as acceleration factors during testing. Accelerated temperature and voltages are not set to a point that would damage the device, thereby causing a failure that would not occur under normal operating conditions. During high temperature operating life testing, the devices are subjected to 125°C at an internal voltage of V_{CC} + 0.4V. Afterward, extrapolation from accelerated conditions to nominal conditions is possible.

Temperature Acceleration Factor

The Arrhenius equation, shown below, is used to statistically predict and model the accelerations factor due to temperature.

$$AF_T = e^{\frac{E_A}{k}\left(\frac{1}{T_O} - \frac{1}{T_S}\right)}$$

Arrhenius Equation

k = Boltzmann's constant = 8.617 x 10^{-5} eV/K
T_O = Operating temperature in kelvins
T_S = Stress temperature in kelvins
E_A = Activation energy for respective failure mechanism

The stress temperature (T_S) used to collect data is 125°C. T_O is the normalized operating temperature. All temperature data is converted into degrees kelvin. Boltzmann's constant, illustrated as *k* in the Arrhenius equation, is equal to 8.617×10^{-5}eV/K. The activation energy (E_A), expressed in electron volts (eV), is a function of the temperature dependence on the failure mechanism. The lower the E_A, the less influence the temperature has on the failure mechanism. E_A is derived through experimental stress data collected at burn-in over time that is common among all semiconductor devices. In the case of DRAM, the most relevant activation energy is due to the time-dependent dielectric breakdown (TDDB). When T_O is equal to T_S, the acceleration factor due to temperature is equal to 1. As seen by the Arrhenius equation, temperature has an exponential effect on the long-term reliability of all CMOS-based ICs.

Voltage Acceleration Factor

The second acceleration factor used in long-term reliability testing is voltage. The voltage acceleration factor is shown below. Voltage stress is independent of the operating voltage specified in the data sheet in most cases. Most DRAM devices internally regulate the voltage down to an internal operating voltage, V_{CC}, of the given process. During the high-temperature operating life test and burn-in, the regulators are disabled with the voltage moved to V_{CC} + 0.4V as a stress voltage. The constant (β) is determined experimentally in relation to TDDB, representing the slope in relation to the time between a

failure versus the stress voltage. β is primarily dependent on the thickness of the gate oxide used in the manufacturing process. As shown by this model, voltage is also exponentially related to the reliability of CMOS devices.

$$AF_V = e^{\beta(Vs - Vo)}$$

Voltage Acceleration Factor

β = Constant, the value is derived experimentally
V_s = Stress voltage
V_o = Operating voltage

Overall Acceleration Factor

The overall acceleration factor (AF_{OA}, shown below) is calculated as the product of the two respective acceleration factors (temperature and voltage). The AF_{OA} shows the relationship from the stress conditions using unregulated voltages to nominal conditions as seen in the system.

$$AF_{OA} = AF_V \times AF_T$$

Overall Acceleration Factor

Failure Rate Calculation

The failure rate of an IC can be expressed in many different ways, but once you have the data, it is not difficult to convert the data into the desired format. Assuming that failures occur as random independent events, component failure rates can be calculated using the equation below. The three components used to predict the final failure rate are Poisson statistic, device hours tested, and the number of failures in the sample size being tested.

$$\text{Failure rate} = \frac{Pn}{\text{Device hours at accelerated environment} \times AF_{OA} \text{ relative to system operating conditions}}$$

Failure Rate Calculation

The Poisson statistic used in this equation, P_n, is derived from the Poisson probability distribution equation shown in the figure below (Poisson Probability Distribution Equation). P_r in the equation represents 1 minus the confidence level at which the failure rate is calculated. In the equation, *r* represents the total number of fails in the sample size. After P_r and *r* are defined, you can solve for P_n.

Calculating the Poisson statistic can be difficult without a statistics calculator, but the values used in the Poisson curves can be estimated, as seen in Figure 2. C represents the number of fails in the sample size, and P_a represents 1 minus the confidence level. Drawing a horizontal line from the P_a value until it intersects the curve, C, equals the Poisson statistic. The P_n value can then be determined by dropping a vertical line down from the intersection. The confidence levels of 60% and 90% are shown based on zero fails in the sample size.

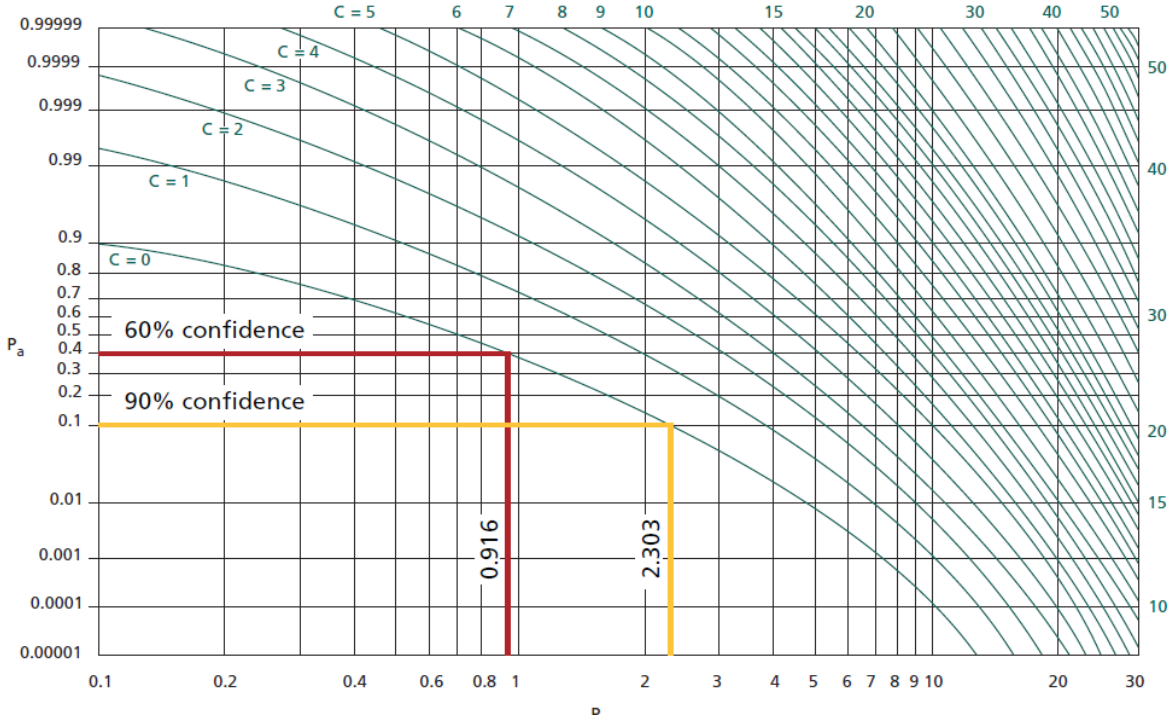
Table 2 shows the Poisson statistic based on the number of fails versus the confidence levels set at 60% and 90% from 0 to 5 failures. Micron uses a 60% confidence level for all failure rate calculations published for DRAM devices. If a higher level of confidence is needed, recalculating this can be done using a different P_n to represent the desired confidence level.

$$P_r = \sum_{i=0}^{r} \frac{(e^{-Pn} Pn^r)}{(i!)}$$

Poisson Probability Distribution Equation

P_r = One minus the confidence level at which the failure rate is calculated
r = The total number of failed devices from our test samples

Figure 2: Poisson Curves



Note: 1. C = Acceptable number of failures in the sample.

Table 2: Poisson Statistic

Number of Fails	60% Confidence Level	90% Confidence Level
0	0.916	2.303
1	2.022	3.890
2	3.105	5.322
3	4.175	6.681
4	5.237	7.994
5	6.291	9.275

The total device hours tested under the stress conditions is relatively straightforward. For this part of the equation, the total number of devices is multiplied by the total amount of time in the high temperature operating test. The total number of fails obviously affects the final reliability calculation, but so does the time of the fail. Early failures have a greater effect on the final result than do fails later in the test flow. This is because early failures reduce the total number of device test hours more than failures that happen later in the test flow. For example, if the sample size is 100 throughout the testing and each device is tested for 1008 hours, the total device hours equates to 100 × 1008 or 100,800 hours of device operation.

The final element of the failure rate calculation is the overall acceleration facture due to temperature and voltage as discussed earlier. This acceleration factor is where the tem-

perature can be varied to determine the failure rate based on a nominal voltage and temperature.

After the failure rate is calculated, it can be expressed in two formats: failures per billion device hours (FIT) or the percentage of failures per thousand device hours. To convert the failure rate calculation into a FIT rate, the value needs to be multiplied by 10^{+9}, and to convert this into a percent failures per thousand device hours, the value is multiplied by 10^{+5}. The failure rate at Micron is expressed in failures per billion device hours, FIT.

To determine the total system FIT rate, the calculated FIT rate for a given IC is multiplied by the number of DRAM devices in the system. For example, if the FIT rate for a single component is 10, a system using 4 DRAM devices would have a total system FIT rate of 40 FIT. As mentioned earlier, this is the reason that the number of DRAM used in the system is crucial to overall system reliability.

Applying the Reliability Data to System Use Conditions

With the reliability statistics described in the previous sections, predicting the system FIT rate at a given confidence level is relatively straightforward. FIT can be calculated by replacing the T_O value in the temperature acceleration factor with the sustained operating temperature of the system along with the number of devices. Deriving the mean time between failure (MTBF) from the system FIT can be done using the equation below, where *n* is the number of components in the system. The units for MTBF calculation are hours of use.

$$MTBF = \frac{1}{n \times FITs \times 10^{-9}}$$

Mean Time Between Failure

System Rate FIT Example

The following equation is an example of the system FIT rate for a 256Mb SDRAM device for an application running at 105°C.

$$AF_T = e^{\frac{0.6}{8.617 \times 10^{-5}}\left(\frac{1}{378} - \frac{1}{398}\right)} = 2.524$$

$$AF_V = e^{5(2.7 - 2.3)} = 7.389$$

$$AF_{OV} = 7.389 \times 2.524 = 18.650$$

System FIT Rate for a 256Mb SDRAM

k = Boltzmann's constant = 8.617×10^{-5} eV/K
T_O = Operating temperature in kelvins
T_S = Stress temperature in kelvins
E_A = Activation energy for respective failure mechanism
β = Constant, the value is derived experimentally
V_S = Stress voltage
V_O = Operating voltage

The table below illustrates the high-temperature operating life data collected for the DRAM device. This data is necessary when calculating the total hours tested and the number of failures in the sample size.

Table 3: DRAM Example Test Data

Sample #	168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1008 Hours
1	0/498	0/498	0/498	0/200	0/200	0/200
2	0/499	0/499	1/499	0/200	0/200	0/200
3	0/499	0/499	0/499	0/200	0/200	0/200

Table 3: DRAM Example Test Data (Continued)

Sample #	168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1008 Hours
Total	0/1496	0/1496	1/1496	0/0600	0/0600	0/0600
Failure Analysis Summary						
Interval	Sample #	No. of Fails				
504 hours	2	1				

The device hours is a simple calculation of the number of devices multiplied by the total number of hours tested, measured in hours:

Device hours = (1496 - 168) + (1496 - 168) + (1496 - 168) + (600 - 168) + (600 - 168) + (600 - 168) = 1,056,384 or $1.056 \times 10^{+6}$

The Poisson statistic is calculated using a single fail in the sample size at a 60% confidence level, as shown below.

$$0.4 = \sum_{i=0}^{1} \frac{(e^{-Pn} Pn^{1})}{(i!)}$$

$$P(n) = 2.022$$

Posson Statistic Calculated at a 60% Confidence Level

The final failure rate and FIT can now be calculated for the operating temperature of 105°C.

$$FR = \frac{2.022}{1.056 \times 10^{6} \times 18.650}$$

$$FR = 1.027 \times 10^{-7}$$

$$FR = 1.027 \times 10^{-7} \times 1.0 \times 10^{9} = 102$$

FR = failure rate

Final Failure and FIT Rates

With the FIT rate calculated, the MTBF can be calculated. In the figure below, we are assuming one device in the system (see Figure 3).

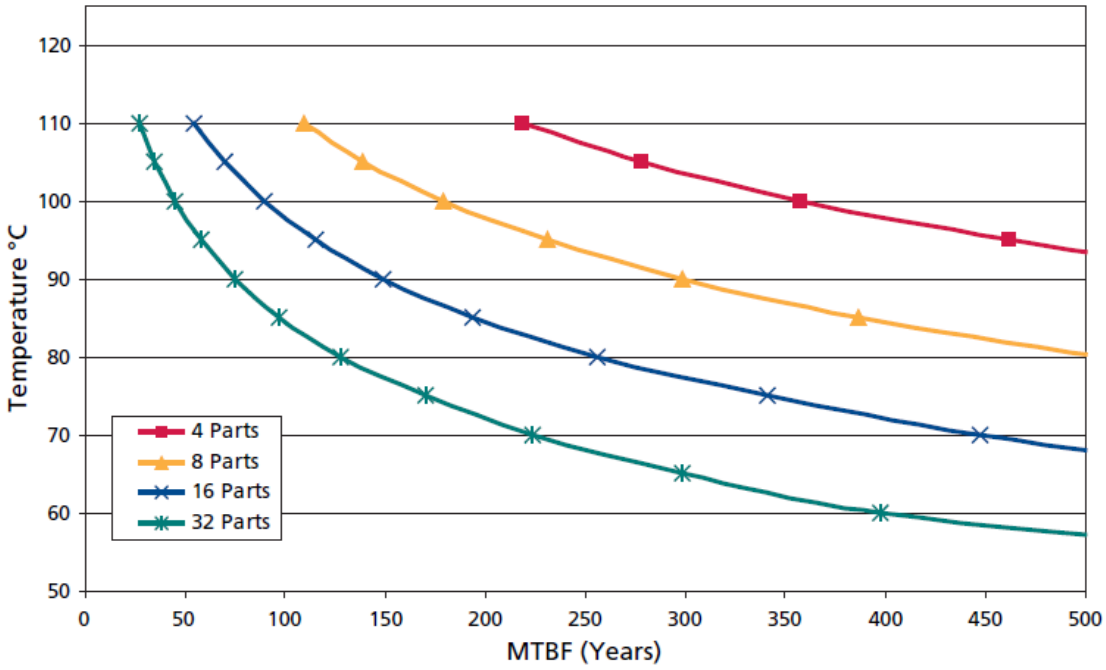
$$MTBF = \frac{1}{1 \times 102 \times 10^{-9}}$$

$$MTBF \approx 9.8 \text{ million hours}$$

$$MTBF \approx 1100 \text{ years}$$

Mean Time Between Failure Calculation

Figure 3: Example of Memory System Mean Time Between Failure for Multiple Micron DRAM Components



Package Reliability

Package reliability is generally not a concern at constant operating temperatures below 125°C. However, reliability predictions can be made if conditions in the use environment are known and acceleration factors are calculated. Data provided by Micron in device qualification reports or acquired by applying knowledge of expected failure mechanisms in the use environment can be used to calculate the acceleration factors.

The Hallberg-Peck acceleration model is commonly used for temperature and humidity stress.

$$AF = \left(\frac{RH_s}{RH_O}\right)^3 \times e\left[\left(\frac{E_A}{k}\right) \times \left(\frac{1}{T_O} - \frac{1}{T_s}\right)\right]$$

Hallberg-Peck

where:

E_A = Activation energy of defect mechanism (0.9 commonly used)
Boltzmann's constant (k) = 8.617×10^{-5} eV/K
RH_s = Stress test environment relative humidity
RH_O = Operating use environment relative humidity
T_s = Stress test environment temperature
T_O = Operating use environment temperature

Two common acceleration models are used to calculate thermal cycling stress:

$$AF = \left(\frac{\Delta T_s}{\Delta T_O}\right)^m$$

Coffin-Manson

$$AF = \left(\frac{\Delta T_s}{\Delta T_O}\right)^{\tilde{1.9}} \times \left(\frac{F_O}{F_S}\right)^{1/3} \times e^{[0.01 \times (T_S - T_O)]}$$

Modified Coffin-Manson (SnPb Solder Joints)

where:

m = Exponent dependent on defect mechanism and material
ΔT_s = Stress test thermal cycle temperature change
ΔT_O = Operating use thermal cycle temperature change
F_O = Operating use thermal cycling frequency
F_s = Stress test thermal cycling frequency
T_s = Maximum temperature during stress test thermal cycle
T_O = Maximum temperature during operating use thermal cycle

Summary

When exceeding the specified device temperature limits, a customer faces three concerns. First, the functionality and performance of the device must be considered, and the system design must be adjusted accordingly. Second, device reliability is reduced, which can be calculated using the proper reliability equations. Finally, temperatures below +125°C are not a concern for package reliability, but temperature cycling can be a concern and should be avoided.

Uprating can be performed on many levels. For instance, the military—through its COTS program—buys commercially rated semiconductors and re-evaluates device suitability for its temperature-rated applications. This can be accomplished using a variety of methods, including common practices of parameter conformance, parameter re-characterization, stress balancing, and higher assembly level testing[13]. However, these processes are very expensive and add to the cost of the components[18]. At the other extreme, a user could simply take commercially rated devices, assess their critical function parameters and decreased reliability, and simply design the system around these issues.

Many semiconductor manufacturers design significant margin into their products. However, semiconductor manufacturers who provide products for multiple temperature specification ranges, as Micron does, generally do not have different device fabrication processes based on the expected temperature range of the application. For example, commercial and industrial devices are generally from the same fabrication process and, therefore, have equivalent intrinsic device reliability. The primary difference is that the industrial devices have been screened for data sheet functionality at the necessary temperature extremes[13].

Before products are uprated, a thorough understanding of the thermal environment is needed. Uprating can be an expensive process. If devices are never subjected to extended temperatures, there is probably no reason to add the costs associated with uprating, even if the system has been specified to extended temperatures. For details on thermal measurements, see Micron's Thermal Application Technical Note (TN-00-08).

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Revision History

Rev. G – 2/2020

- Updated Introduction, Device Functionality, and Failure Rate Calculation sections.
- Updated template.

Rev. F – 5/10

- Updated Table 1, "Junction Temperature, Functionality," on page 2.

Rev. E – 5/08

- Updated Table 1, "Junction Temperature, Functionality," on page 2.

Rev. D – 1/07

- Updated Table 1, "Junction Temperature, Functionality," on page 2.
- Edited for readability.
- Corrected Table 2, "Industry-Standard Typical Junction Temperature Limits", on page 2, Under the hood temperature to -40-150.

Rev. C – 11/06

- Updated "Device Reliability" section
- Added "Long-Term Reliability", "Temperature Acceleration Factor", "Overall Acceleration Factor", "Failure Rate Calculation", and "Applying the Reliability Data to System Use Conditions" sections.

Rev. B – 11/05

- Updated template.
- Corrected typos: Equation 2 on page 2, TN-00-08 reference on page 10, and Boltzmann's constant from 8.6171 to 8.6174 on page 10.

Rev. A – 10/04

- Initial release

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