Technical White Paper

Powering a New Era of High-Performance Space-Grade Xilinx FPGAs

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ABSTRACT

Today's space industry is undergoing an unprecedented expansion across numerous dimensions. There is a rapid increase in the number of spacecraft deployed either in low-earth orbit, mid-earth orbit or geosynchronous orbit. An ever-expanding number of spacecraft includes advanced architectures that deliver a plethora of new scientific instruments.

For many systems, power is now the No. 1 design constraint, as the migration to higher levels of performance and smaller form factors make designing within the same or even lower power budgets more challenging.

Xilinx's 20-nm Kintex UltraScale™ XQRKU060 radiation-tolerant field-programmable gate arrays (FPGAs) are powerful enough to enable entirely new system architectures. The XQRKU060's ability to support in-flight reprogrammable systems gives satellite operators the ability to potentially reconfigure the basic functionality of the satellite, which is not possible in today's fixed-function implementations. Beyond adding a new level of flexibility, the XQRKU060 enables increased data throughput, which helps reduce the costs of transporting data. These new architectures are also capable of supporting artificial intelligence applications, enabling the satellite to locally process an image or radar data without the normal requirement of ground-based review, thus improving mission responsiveness and real-time processing.

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1 Powering the XQRKU060: Key Challenges

As a result of its high performance, depending on its programmed capabilities (clock frequency, logic usage), the total on-chip power required for an FPGA could be as high as 30 W. The core voltage of the chip, VCCINT, needs a large percentage of this power. At about 0.95-V nominal (see the XQRKU060 data sheet and Xilinx Power Estimator [XPE] for exact values), depending on the bitstream deployed, this power could translate to more than 25 A of current. Additionally, because of the advanced XQRKU060 process-node technology, the VCCINT voltage electrical tolerance requirements are tight; this tolerance includes electrical performance as well as radiation effects. Therefore, powering up devices like the XQRKU060 requires a different approach to meet the tolerances for successful operation of the device. Let's separate these challenges into DC and AC regulation.

2 DC Regulation

One obvious factor related to DC regulation is the DC setpoint accuracy of the converter supplying VCCINT. This DC accuracy depends on factors such as the accuracy of the converter's internal reference, the passives used with the converter (such as feedback resistors) and the layout of the printed circuit board (such as ohmic drops). From these factors, the internal reference of the converter represents a large percentage of the voltage accuracy specified by the FPGA manufacturer. However, you should calculate the accuracy of the internal reference in a way that is representative of the application.

As an example, temperature heavily influences the voltage drift of a reference; thus, you should calculate the accuracy for the temperature range to which the devices will be exposed during the mission. Typically, this range is from –40°C to +90°C, which is smaller than the standard military temperature range of –55°C to +125°C used to characterize space-rated devices. The TPS7H4001-SP from Texas Instruments has an internal reference with ±1.5% accuracy across electrical and radiation conditions for the entire military temperature range. A simple calculation of the temperature coefficient (0.1 mV/°C) reveals that in the actual application (–40°C to +90°C), the accuracy of the internal reference is about ±1.1%. You must also take into account radiation effects that could potentially affect DC regulation.

DC regulation typically refers only to the DC setpoint accuracy of the converter supplying VCCINT. The XQRKU060, as well as the converters that provide its power, is offered in a ceramic package because of its use in space applications. While ceramic packages offer hermeticity, they also present unique challenges not encountered in commercial-rated devices, including a larger footprint and larger resistance given the materials used in the package. In the case of the XQRKU060, the effect of ceramic package resistance in DC regulation is larger as the current increases, and the current will depend on the bitstream used. To mitigate this larger resistance, the XQRKU060 offers two pins, VCCINT_SENSE and GND_SENSE. Figure 2-1shows the connections needed between the TPS7H4001-SP and the XQRKU060 sensing pins, as well as a simple representation of the internal package resistance for VCCINT and GND.

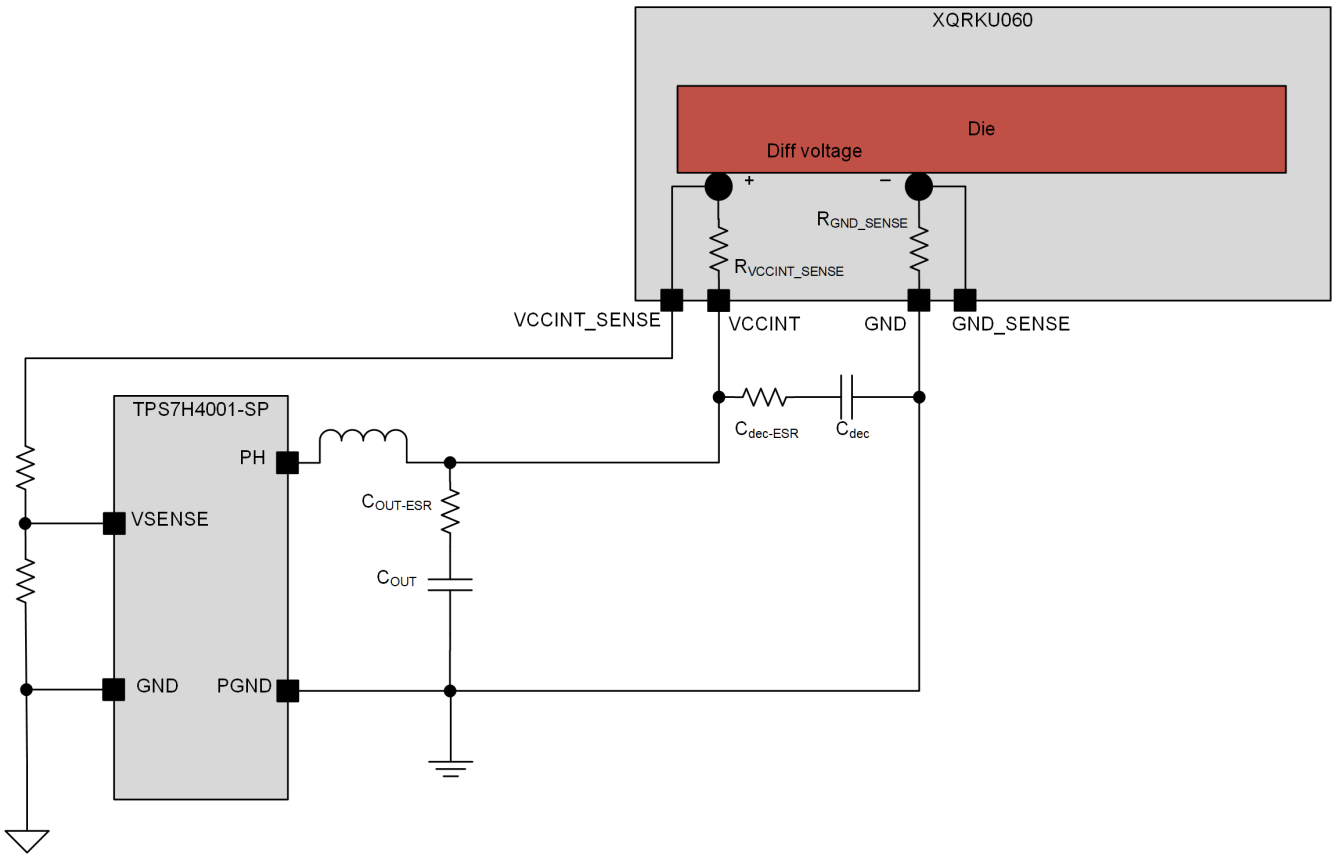

Figure 2-1. XQRKU060 Sensing Connections to the TPS7H4001-SP

Because the TPS7H4001-SP does not offer a GND sensing pin, using only the VCCINT_SENSE pin in the XQRKU060 for the feedback signal (VSENSE) compensates for the voltage drop created by the package resistance RVCCINT_SENSE, as shown in Figure 2-1. If you don't use the GNDSENSE pin for regulation, there is a small resistance that you need to account for. XPE provides the exact value for VCCINT to account for this small resistance. If not used, you can route the GNDSENSE pin to an optional test point or leave it floating, as indicated in the XQRKU060 data sheet.

As the current supplied by the TPS7H4001-SP increases, the internal differential voltage across the XQRKU060 die might decrease, depending on the internal RGND_SENSE resistance. Figure 2-2 shows the relationship between VCCINT current and the different pin voltages for two different assumed values of internal package resistance. Both cases assume a nominal VCCINT voltage of 0.95 V.

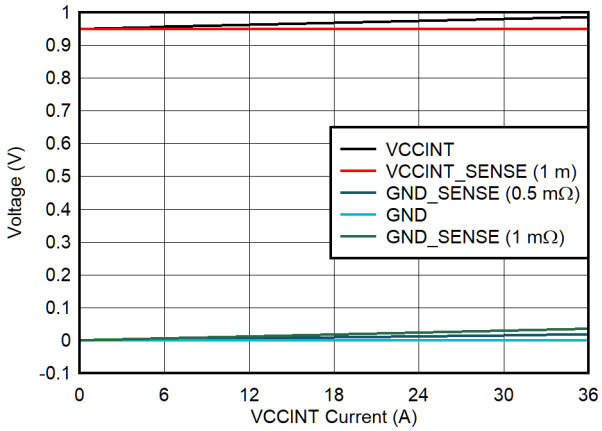

Figure 2-2. Voltages at the XQRKU060 Pins as a Result of Sensing Pins

The first scenario in Figure 2-2 assumes the same resistance value of 1 mΩ for both R_{VCCINT_SENSE} and R_{GND_SENSE}. In this case, you can see how the VCCINT_SENSE voltage remains constant at 0.95 V (dotted red line), while the GND_SENSE voltage (dotted black line) increases as the VCCINT current increases.

GND signals and planes are typically the least resistive in ceramic packages given the large number of pins and planes used. Therefore, Figure 2-2 also shows an example where R_{VCCINT_SENSE} = 1 mΩ but R_{GND_SENSE} = 0.5 mΩ. In this particular case, the increase in the GND_SENSE voltage (dotted blue line) as the VCCINT current increases is much less than when R_{GND_SENSE} = 1 mΩ. It is important to reemphasize that when using XPE, even this low R_{GND_SENSE} value is compensated in the exact VCCINT value indicated.

Figure 2-3 shows the impact of these two scenarios in the differential voltage across the XQRKU060 die. You can see that when R_{VCCINT_SENSE} = R_{GND_SENSE} = 1 mΩ, the differential voltage across the XQRKU060 die decreases to 0.914 V as the VCCINT current reaches 36 A. When R_{VCCINT_SENSE} = 1 mΩ but R_{GND_SENSE} = 0.5 mΩ, however, the differential voltage only decreases to 0.932 V as the VCCINT current reaches 36 A. While the 18-mV difference between these two scenarios might seem low, this translates to a 3.7% (VCCINTdiff = 0.914 V) vs. a 1.9% (VCCINTdiff = 0.932 V) DC-regulation tolerance (from 0.95-V nominal), which is significant in the context of VCCINT voltage tolerance requirements.

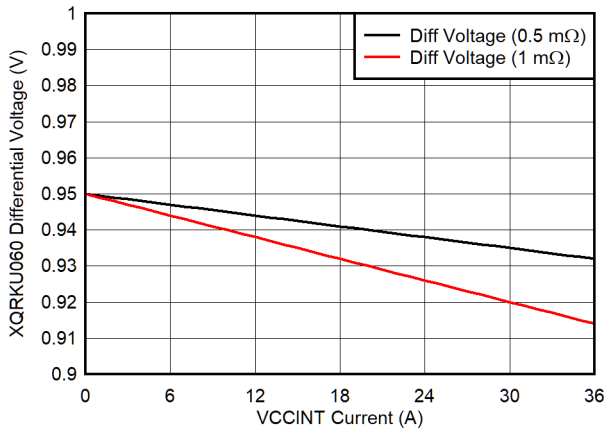

Figure 2-3. Differential Voltage Across the XQRKU060 for Two Different R_{GND_SENSE} Values

3 AC Regulation

AC regulation is associated with load transients in the VCCINT rail. These load transients depend heavily on the programming code used in the FPGA. Consequently, we recommending writing the code in a way that avoids severe transients as much as possible – in other words, avoid enabling a large amount of logic in the FPGA at once. Load transients are always present, however, you need to properly address them to meet the regulation requirements.

Given the nature of some of these transients (some with high slew rates in the ampere-per-nanosecond range), the converter might not respond to the voltage drop caused by the transient quickly enough. This is where the decoupling capacitors recommended by Xilinx become critical (see the XQRKU060 data sheet for detailed information regarding decoupling capacitors for different transient scenarios). These decoupling capacitors are in addition to any internal decoupling capacitors typically included in FPGA packages. Figure 3-1 shows an example of an approximately 7-A load transient in the microseconds range.

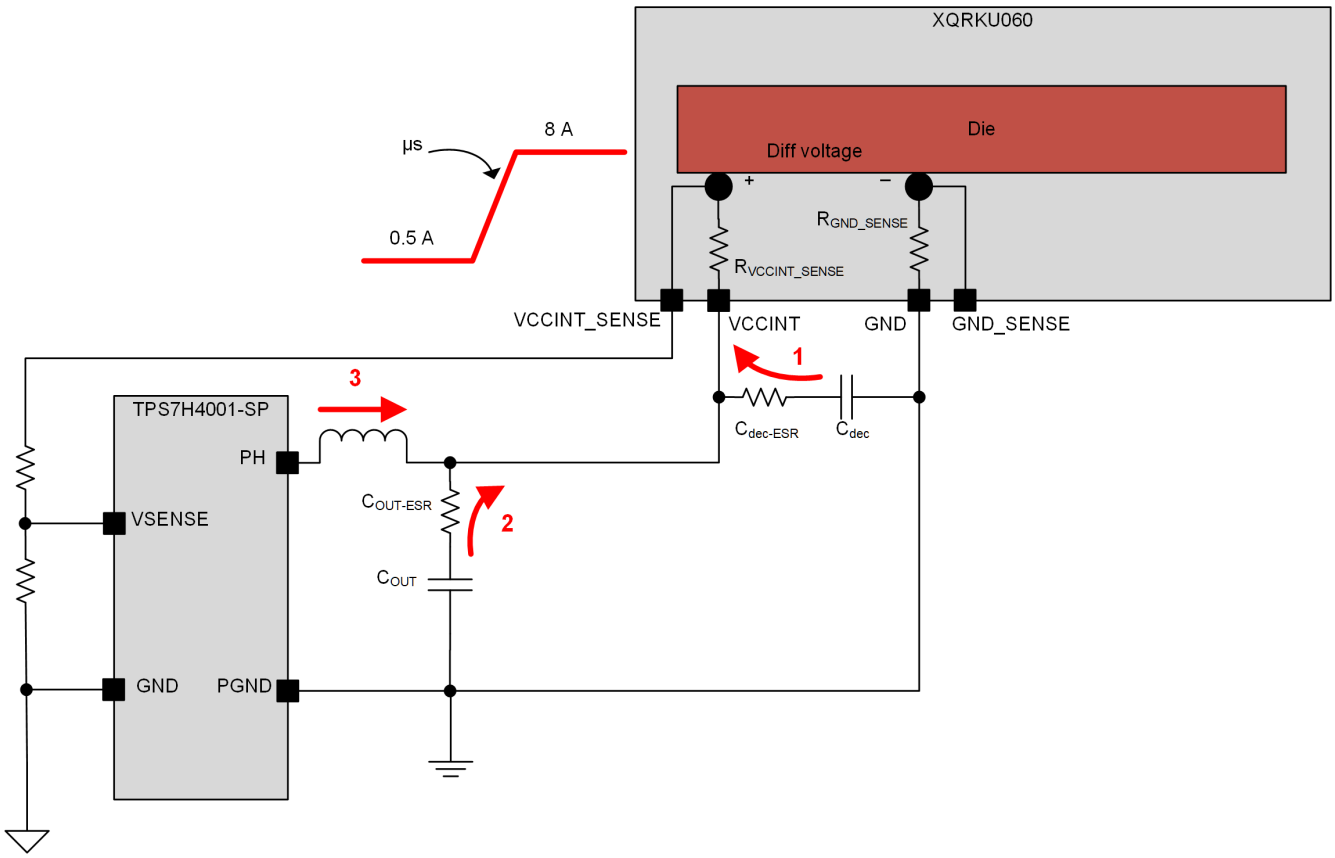

Figure 3-1. AC Regulation Response Due to Load Transients

Initially, the internal and external decoupling capacitors will respond to the current increase. The external decoupling capacitors are sized to match the worst-case expected transient based on the XQRKU060 data sheet recommendation and, as a result, they will handle the transient properly. In case the FPGA still requires additional current after the depletion of the decoupling capacitors, the output capacitors of the converter will supply current until the converter is able to respond. You must choose the crossover frequency of the converter and the respective feedback compensation accordingly for every application.

4 Radiation Effects

Along with DC and AC regulation, we recommend you consider any radiation effects introduced by the converter to meet the tolerance requirements from the XQRKU060. These radiation effects include total ionizing dose (TID) and single-event transients (SETs).

TID could introduce drift in the internal reference of the converter that could affect DC regulation. The TPS7H4001-SP is rated up to 100 krad(Si), and Texas Instruments tests every specification to meet the data sheet limits after exposure to 100 krad(Si). The internal reference of the TPS7H4001-SP shows very little sensitivity to TID, with a maximum drift of 2 mV (~0.3%) at 100 krad(Si).

Transients induced by heavy ions (SETs) are not as predictable as TID and could have a very negative effect on regulation. A converter sensitive to transients that shuts down the output of the converter or exceeds the maximum regulation requirements of the XQRKU060 could severely compromise the performance of the FPGA. Additionally, large and positive transients could potentially damage the FPGA.

The TPS7H4001-SP is fully characterized for SETs up to a linear energy transfer (LET) equal to 75 MeV-cm2/mg and shows resilient performance with a low number of SETs (<10 at PVIN = 5 V, VIN = 5 V) when the output voltage exceeds ±3% at a fluency of 10 million ions/cm2 (see the Single Events Effects Test Report of the TPS7H4001-SP for details). This translates to a very low SET cross-section of 2.18 × 10-7 cm2/device (PVIN = 5 V, VIN = 5 V). This SET performance, along with its TID rating of 100 krad(Si), makes the TPS7H4001-SP a reliable converter to power up the XQRKU060.

5 ADA-SDEV-KIT2 Platform

With the ADA-SDEV-KIT2 platform from Alpha Data Parallel Systems, you can evaluate the KU060 (the commercial package) alongside a space-rated power solution from Texas Instruments. The platform also allows you to test the interaction of the KU060 with other devices (such as high-speed analog-to-digital converters) through its FPGA mezzanine card connectors. Figure 5-1 shows a picture of the ADA-SDEV-KIT2.

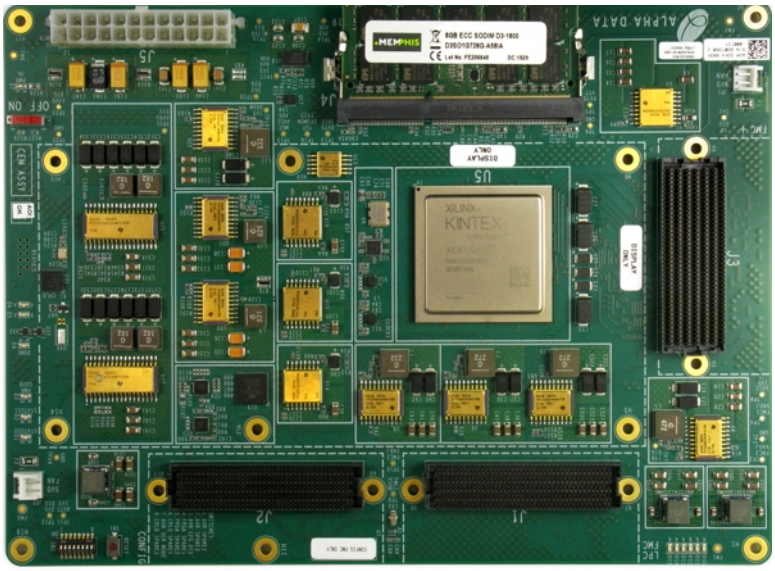

Figure 5-1. The ADA-SDEV-KIT2 Platform for the KU060

To test the performance of the TI-based power supply on the ADA-SDEV-KIT2 platform, Texas Instruments and Alpha Data Parallel Systems performed a large amount of testing using a modified version of the ADA-SDEV-KIT2 kit that used the XQRKU060 (ceramic package) instead of the KU060 (commercial package).

The testing focused on two aspects:

- Assessing the behavior of the XQRKU060 ceramic package and correlating it to the expectations of the GND pins resistance discussed in this paper.
- Validating the approach shown in Table 5-1 (nonuse of the GND_SENSE pin) in DC and AC conditions.

To validate the first aspect, the testing focused on measuring the GND_SENSE pin voltage using two different bitstreams to calculate RGND_SENSE. The bitstreams were generated in a way that the FPGA would require a current from the VCCINT rail large enough to generate a voltage at the GND_SENSE pin. Table 5-1 lists the main features for these two bitstreams. All of the measurements were in DC conditions.

Table 5-1. Bitstreams Used to Evaluate the XQRKU060 in the ADA-SDEV-KIT2

		Bitstream No. 1	Bitstream No. 2
Clock rate		13%, 150 MHz	7%, 200 MHz
Logic usage		81%	24%
Block random access memory usage		0	47%
Digital signal processor usage		0	19%
Gigabit transceiver usage		0	0%
Peak VCCINT core current		≅9 A	≅25 A
XPE VCCINT voltages	Minimum	0.917 V	0.922 V
	Maximum	0.993 V	0.998 V

For the resistance calculations, the COMP pin voltage in the TPS7H4001-SP approximated the current corresponding to each bitstream shown in Table 5-1, approximately 9 A and 25 A. The COMP pin voltage correlates to the peak output current from the power stage of the device. These current approximations

were also very closely aligned with the VCCINT and VCCINT_IO currents obtained from XPE (VCCINT and VCCINT_IO are internally connected in the XQRKU060, as indicated in the data sheet).

The data after this testing resulted in RGND_SENSE values of 0.25 mΩ and 0.36 mΩ for the approximately 9-A and 25-A bitstreams, respectively. This agrees with the expectations that GND signals and planes are typically the least resistive in ceramic packages given the large number of pins and planes used.

All tested cases met the DC regulation requirements for the VCCINT in the XQRKU060, as validated by XPE and Vivado software.

Writing bitstream No. 1 into the external configuration flash memory of the ADA-SDEV-KIT2 validated the AC regulation. The FPGA was cleared and then configured from the flash memory in a constant loop. The DONE signal from the FPGA connected to a diode was used as a trigger to capture the AC transients.

The signals captured were VCCINT, GND, VCCINT_SENSE and GND_SENSE. The first two signals were captured across a decoupling capacitor under the FPGA. The SENSE signals were captured using 0-Ω resistor footprints (not populated for the ceramic package version of the KU060) under the FPGA that provided connection to the VCCINT_SENSE and GND_SENSE pins. For reference, Table 5-2 lists the VCCINT decoupling capacitors used in the ADA-SDEV-KIT2. This capacitance does not include the decoupling capacitors used for the TPS7H4001-SP.

Table 5-2. VCCINT Decoupling Capacitors Used in the ADA-SDEV-KIT2

Capacitor value (µF)	Quantity
680	3
100	5
47	13
4.7	10
1	16
0.22	55

While in the unprogrammed state, the VCCINT rail in the ADA-SDEV-KIT2 FPGA consumes approximately 0.5 A. This means that each time the FPGA was either configured or cleared, approximately a 8.5-A transient would occur.

Figure 5-2 shows scope shots of the VCCINT response with respect to GND, while Figure 5-3 shows scope shots of the VCCINT_SENSE response with respect to GND_SENSE. In both cases, the load-step responses meet the ±38-mV regulation requirement from XPE as shown in Table 5-1 (0.917 V-0.993 V).

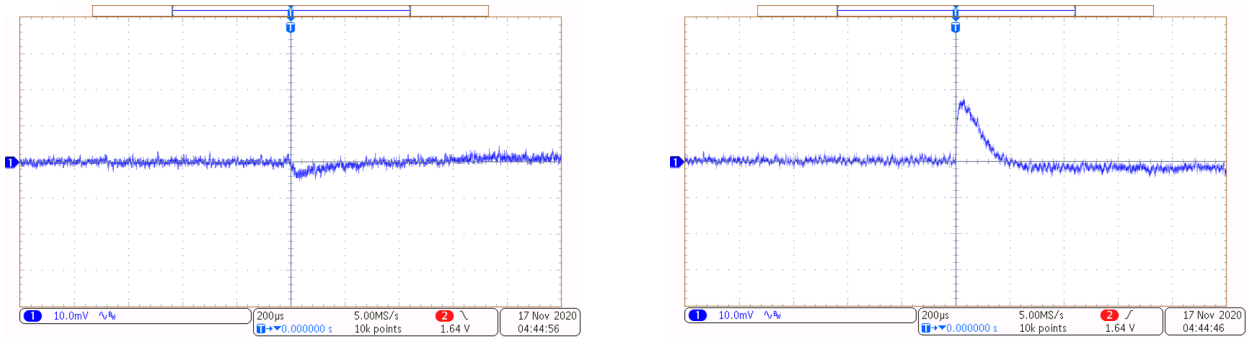

Figure 5-2. VCCINT transient response with respect to GND using bitstream No. 1 in the ADA-SDEV-KIT2. The response on the left represents the increasing load step and the response on the right represents the decreasing load step.

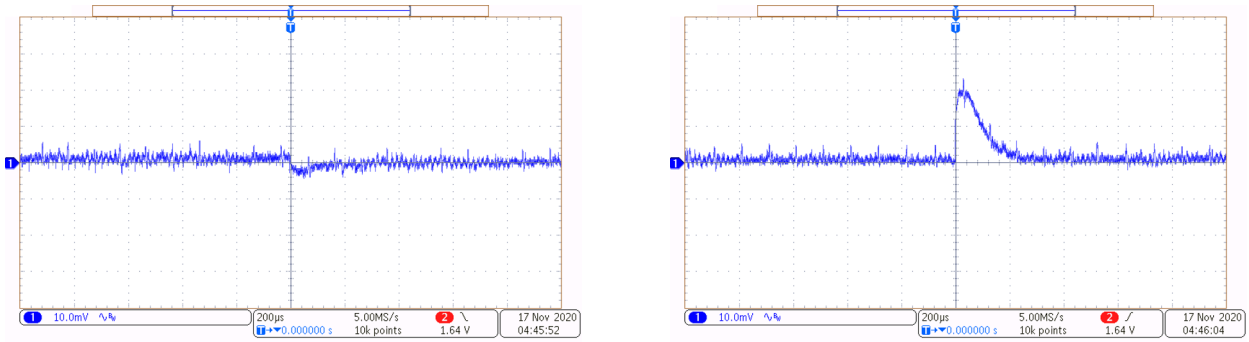

Figure 5-3. VCCINT_SENSE transient response with respect to GND_SENSE using bitstream No. 1 in the ADA-SDEV-KIT2. The response on the left represents the increasing load step and the response on the right represents the decreasing load step.

6 Conclusion

The XQRKU060 is a high-performance FPGA for space applications that is enabling new system architectures in a rapidly evolving market. Given its advanced computing capability, powering up the XQRKU060 requires considering multiple scenarios and constraints in order to meet its voltage regulation requirements. These scenarios include DC and AC regulation as well as radiation effects. By configuring the output voltage of the TPS7H4001-SP to the specific voltage indicated by XPE, along with the VCCINT_SENSE pin connection, you can be confident in obtaining a robust and validated radiation-hardened power supply.

7 Key Contributors

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